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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,413	SAXE ET AL.	
	Examiner	Art Unit	
	KENNETH TANG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-28,54-56 and 82-135* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-28,54-56 and 82-135* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 26-28, 54-56, and 82-135 are presented for examination.

2. This action is in response to the Amendment on 12/22/09. Applicant's arguments were fully considered but are moot in view of the new grounds of rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 26-28, 54-56, and 82-135 are rejected under 35 U.S.C. 103(a) as being obvious over Knauerhase et al. (US 2004/0268347 A1) (hereinafter Knauerhase) in view of Tovinkere (US 2004/0199919 A1).

4. As to claim 26, Knauerhase teaches a method performed by an operating system executing within a computer system having different types of physical processing modules, the method comprising (Abstract, [0020]):

receiving a first set of parametric information pertaining to a first physical processing module (PPM) (first of a multiple of hyperthreaded processors) ([0020]);

receiving a second set of parametric information pertaining to a second PPM, wherein the second PPM has a different architecture than the first PPM (second of a multiple of hyperthreaded processors) ([0020]);

constructing a first abstraction of the first PPM based, at least partially, upon the first set of parametric information ([0005], [0032], [0034], [0045]), the first abstraction comprising operational information indicating one or more operational characteristics (via processor profile) of the first PPM ([0050], [0052], [0061], [0062]); and

constructing a second abstraction of the second PPM based, at least partially, upon the second set of parametric information ([0005], [0032], [0034], [0045]), the second abstraction comprising operational information indicating one or more operational characteristics (via processor profile) of the second PPM ([0050], [0052], [0061], [0062]);

wherein the second abstraction is different from the first abstraction to reflect the different architecture of the second PPM ([0034], [0035], [0049], [0070], and lines 9-13 of [0076]).

5. As shown above, Knauerhase's plurality of hyperthreaded processors utilize a processor profile and VM profile, which contain data and characteristics for each respective processor and virtual processor ([0050], [0052], [0061], [0062]). However, Knauerhase's profile does not include an indication of how many logical processing entities are provided by the PPMs (or hyperthreaded processors). Tovinkere teaches a plurality of hyperthreaded processors (Fig. 2, item 104) that determine the total number of processing entities, such as threads, for each processor (see Abstract, [0028], [0031], [0032]). Knauerhase and Tovinkere are analogous art because they are both in the same field of endeavor of computer processing with a plurality of hyperthreaded processors. One of ordinary skill in the art would have known to modify Knauerhase's hyperthreaded multiprocessor system such that it would determine the number of logical processing entities (threads) for each processor, as taught in Tovinkere's hyperthreaded

multiprocessor system. The suggestion/motivation for doing so would have been to provide the predicted result of improving the scalability of processors in the hyperthreaded multiprocessing system ([0007]). Therefore, it would have been obvious to one of ordinary skill in the art to combine Knauerhase with Tovinkere to obtain the invention of claim 26.

6. As to claim 27, Knauerhase ([0005], [0032], [0034], [0045]) in view of Tovinkere ([0028], [0031]) teaches wherein the first PPM comprises a first physical processing core which supports a single hardware thread, wherein the second PPM comprises a second physical processing core which supports a plurality of hardware threads, wherein constructing the first abstraction comprises indicating the first physical processing core as a single logical processing entity, and wherein constructing the second abstraction comprises indicating the second physical processing core as a plurality of logical processing entities.

7. As to claim 28, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein constructing the second abstraction comprises indicating that the plurality of logical processing entities corresponding to the second physical processing core share one or more resources of the second PPM.

8. As to claim 54, it is rejected for the same reasons as stated in the rejection of claim 26. In addition, Knauerhase discloses a computer readable storage medium carrying instructions for the method ([0025]).

9. As to claims 55-56, they are rejected for the same reasons as stated in the rejections of claim 27-28, respectively.

As to claim 82, it is rejected for the same reasons as stated in the rejection of claim 26.

10. As to claims 83-84, they are rejected for the same reasons as stated in the rejections of claim 27-28, respectively.

11. As to claim 85, Knauerhase ([0005], [0032], [0034], [0045]) in view of Tovinkere ([0028], [0031]) teaches wherein the first PPM has an n number of processing cores, where n is an integer greater than one, each of the n processing cores capable of supporting one hardware thread; and wherein the second PPM has a single processing core capable of supporting an m number of hardware threads, where m is an integer greater than one.

12. As to claim 86, Tovinkere teaches wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an m number of logical processing entities ([0028], [0029], [0016]).

13. As to claim 87, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein

the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the m logical processing entities of the second PPM.

14. As to claim 88, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share a cache, and wherein the resource sharing information of the second abstraction indicates that the m logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

15. As to claim 89, it is rejected for the same reasons as stated in the rejection of claim 85.

16. As to claim 90, Knauerhase ([0005], [0032], [0034], [0045]) in view of Tovinkere ([0028], [0031]) teaches wherein the first abstraction indicates that the first PPM provides an n number of logical processing entities, and wherein the second abstraction indicates that the second PPM provides an s number of logical processing entities, where s = m times p.

17. As to claims 91-92, they are rejected for the same reasons as stated in the rejections of claims 87-88.

18. As to claim 93, it is rejected for the same reasons as stated in the rejection of claim 85.

19. As to claim 94, it is rejected for the same reasons as stated in the rejection of claim 90.

20. As to claim 95, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the n logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by at least some of the s logical processing entities of the second PPM.

21. As to claim 96, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the resource sharing information of the first abstraction indicates that the n logical processing entities of the first PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache, and wherein the resource sharing information of the second abstraction indicates that at least some of the s logical processing entities of the second PPM share one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

22. As to claim 97, Knauerhase teaches accessing the first abstraction and/or the second abstraction; and determining, based at least partially upon the operational information in the first abstraction and/or the operational information in the second abstraction, whether to dispatch an execution thread to one of the logical processing entities of the first PPM or one of the logical processing entities of the second PPM to be executed thereby ([0005], [0032], [0034], [0045]).

23. As to claim 98, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the operational information of the first abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the first PPM, and wherein the operational information of the second abstraction includes resource sharing information indicating one or more resources shared by the logical processing entities of the second PPM.

24. As to claim 99, Knauerhase ([0077], [0005], [0032], [0034], [0045]) and Tovinkere ([0002]) teaches wherein determining whether to dispatch an execution thread comprises: determining, based at least partially upon the resource sharing information in the first abstraction and/or the resource sharing information in the second abstraction, whether to dispatch an execution thread to one of the logical processing entities of the first PPM or one of the logical processing entities of the second PPM to be executed thereby.

25. As to claim 100, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the resource sharing information in the first abstraction indicates that the logical processing entities of the first PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

26. As to claim 101, Knauerhase ([0077]) and Tovinkere ([0002]) teaches wherein the resource sharing information in the second abstraction indicates that the logical processing

entities of the second PPM are sharing one or more of the following: a processing core, a data pathway, a translation lookaside buffer, and a cache.

27. As to claims 102-135, they are rejected for the same reasons as stated in the rejections of claims 85-101.

Response to Arguments

28. Applicant's arguments were fully considered but are moot in view of the new grounds of rejections.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Kenneth Tang/
Examiner, Art Unit 2195